

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)

Application Number	10653754
Filing Date	2003-09-03
First Named Inventor	Stephan G. Meier
Art Unit	2131
Examiner Name	Unknown
Attorney Docket Number	5500-97500

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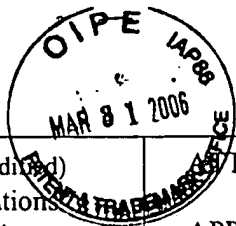
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For Applicant's Information
Disclosure Statement
(Use several sheets if necessary)

PATENT NO. 5500-97500

APPLICANT: Meier, et al.

FILING DATE: September 3, 2003

SERIAL NO. 10/653,754

GROUP: 2131

U.S. PATENT DOCUMENTS

EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
DK		5,412,787	5/95	Forsyth, et al.			
DK		5,813,031	9/98	Chou, et al.			
DK		5,953,748	9/99	Thomas J. Riordan			
DK		6,065,091	5/00	Daniel W. Green			
DK		6,212,602	4/01	Wicki, et al.			

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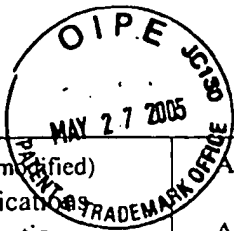
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Information Disclosure Statement--PTO 1449 (modified)

**Form PTO-1449** (modified)

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Disclosure Statement

(Use several sheets if necessary)

ATTY. DKT. NO. 5500-97600

APPLICANT: Shen, et al.

FILING DATE: September 3, 2003

SERIAL NO. 10/653,794

GROUP: 1614

U.S. PATENT DOCUMENTS

EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
DK	B1	6,138,225	10/24/00	Upton et al.			
DK	B2	6,560,679	5/6/03	Choi et al.			

FOREIGN PATENT DOCUMENTS

EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

DK	B3	PCT International Search Report for PCT/US2004/018042 dated March 23, 2005
DK	B4	Choi et al., "A Low Power TLB Structure for Embedded Systems," Computer Architecture Architecture Letters, Vol. 1, January 2002, (4 Pages)
DK	B5	Zhang et al., "Low Cost Instruction Cache Designs for Tag Comparison Elimination," Proceedings of the 2003 International Symposium on Lower Power Electronics and Design, ISLPED'03, August 25, 2003, (Pages 266-269)
DK	B6	Lee et al., "A Selective Filter Bank TLB System," Proceedings of the 2003 International Symposium on Lower Power Electronics and Design, ISLPED'03, August 25, 2003, (Pages 312-317)
DK	B7	Inoue et al., "A History-Based I-Cache for Low-Energy Multimedia Applications," Low Power Electronics and Design, ISLPED'02, August 12, 2002, (Pages 148-153)

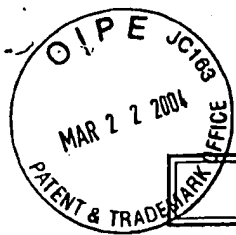
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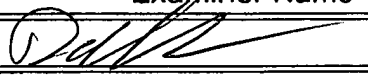
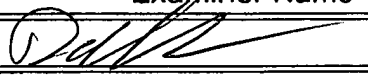
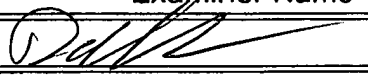
Information Disclosure Statement--PTO 1449 (modified)



ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

Title of Invention	Low Power Way-Predicted Cache																										
<p>Application Number: 10/653754 </p> <p>Confirmation Number: 3663</p> <p>First Named Applicant: Stephan Meier</p> <p>Attorney Docket Number: 5500-97500</p> <p>Art Unit: 2131</p> <p>Search string: (6687789).pn.</p> <p>US Patent Documents</p> <p>Note: Applicant is not required to submit a paper copy of cited US Patent Documents</p> <table border="1"><thead><tr><th>init</th><th>Cite.No.</th><th>Patent No.</th><th>Date</th><th>Patentee</th><th>Kind</th><th>Class</th><th>Subclass</th></tr></thead><tbody><tr><td></td><td>1</td><td>6687789</td><td>2004-02-03</td><td>Keller et al</td><td></td><td></td><td></td></tr></tbody></table> <p>Signature</p> <table border="1"><thead><tr><th>Examiner Name</th><th>Date</th></tr></thead><tbody><tr><td></td><td>12/12/07</td></tr></tbody></table>								init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass		1	6687789	2004-02-03	Keller et al				Examiner Name	Date		12/12/07
init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass																				
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Examiner Name	Date																										
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U.S. PATENT DOCUMENTS

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FOREIGN PATENT DOCUMENTS

EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
DK	A1	0459232	12/4/91	EP			
DK	A2	0259095	3/9/98	EP			
DK	A3	0675443	10/4/95	EP			
FR	A4	2 674 044	9/18/92	FR			
DK	A5	2263987	8/11/93	GB			
DK	A6	2263985	8/11/93	GB			
DK	A7	2281422	3/1/95	GB			
DK	A8	98/20421	5/14/98	WO			
DK	A9	0651321	5/3/95	EP			
DK	A10	0467152	1/22/92	EP			
DK	A11	0381471	8/8/90	EP			

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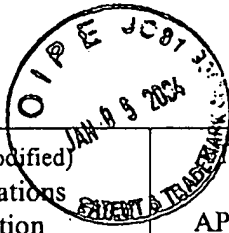
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DK	A13	"Reducing Set-Associative Cache Energy via Way-Prediction and Selective Direct-Mapping," Powell, et al., IEEE, 2001, pp. 54-64.
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DK	A15	"The 16kB Single-Cycle Read Access Cache on a Next-Generation 64b Itanium Microprocessor," ISSCC 2002, Session 6, SRAM and Non-Volatile Memories, 6.6, 2 pages.
DK	A16	XP 000525181 Calder, et al, "Next Cache Line and Set Prediction," Department of Computer Science, University of Colorado, 8345 Computer Architecture News, May 23, 1995, No. 2, pp. 287-296.

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OK	A20	Rupley, et al, "P6: The Next Step?" PC Magazine, September 12, 1995, 16 pages.
OK	A21	Halfhill, "AMD K6 Takes on Intel P6," BYTE Magazine, January 1996, 4 pages.
OK	A22	Patterson, et al, "Computer Architecture: A Quantitative Approach," Section 8.3, pp. 408-425, published by Morgan Kaufmann Publishers, Inc., 1990.
OK	A23	Holstad, S., "Tutorial Tuesday: Decoding MMX" January 14, 1997, Earthlink Network, Inc. copyright 1997, 5 pages (see http://www.earthlink.net/daily/Tuesday/MMX)
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OK	A25	"Intel MMX™ Technology – Frequently Asked Questions" 6 pages (see http://www.intel.com/drg/mmx/support/faq/htm)
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OK	A27	Kessler et al., "Inexpensive Implementations of Set-Associativity," Computer Architecture Conference Proceedings, June 1989, pp. 131-139.

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Title of Invention	Low Power Way-Predicted Cache
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Application Number: 10/653754
 Confirmation Number: 3663
 First Named Applicant: Stephan Meier
 Attorney Docket Number: 5500-97500
 Art Unit: 2131

Search string: (6115792 or 6016533 or 5845323 or 5752069
 or 4912626 or 5509119 or 5091851 or 5210845
 or 5148538 or 5530958 or 5559975 or 6425055
 or 5918245 or 6553477 or 6418521 or 5412787
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 or 4807115 or 4858105 or 5226126 or 5226130
 or 5619676 or 5835951).pn.

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Remarks

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